What is claimed is:

1. A semiconductor memory device, comprising:

km memory cell array blocks arranged in the form of a k×m matrix, divided by x block selecting signals and y block selecting signals, and including a plurality of divided word lines arranged horizontally;

km of xy address word lines arranged above or below the km memory cell array blocks; and

km of divided y address word lines arranged vertically from the km of xy address word lines to the km memory cell array blocks.

2. A semiconductor memory device, comprising:

km memory cell array blocks arranged in the form of a k×m matrix, divided by x block selecting signals and y block selecting signals, and including a plurality of divided word lines arranged horizontally;

a plurality of bit lines for each of the km memory cell array blocks arranged vertically;

a plurality of main word lines for a plurality of bit lines for each of the km memory cell array blocks arranged horizontally;

km of xy address word lines above or below the km memory cell array blocks;

decoding means for decoding a corresponding x block selecting signal among x block selecting signals generated by decoding the x block selecting

address and y block selecting signals generated by decoding the y block address to select corresponding m of xy address word lines and for being arranged for each of m memory cell array blocks arranged horizontally among the km memory cell array blocks;

km of divided y address lines arranged vertically from the km xy address word lines to the km memory cell array blocks; and

word line driving means for combining the plurality of the main word lines of each of the km memory cell array blocks and a signal of a corresponding xy address word line among the km of xy address word lines to select the plurality of the divided word lines and for being arranged for each of the km memory cell array blocks.

3. The device of claim 3, wherein the y block selecting signals are vertically arranged collectively on a right or a left side.

4. A layout method of a semiconductor memory device, comprising:

arranging km memory cell array blocks divided by x block selecting signals and y block selecting signals in the form of a matrix and arranging horizontally a plurality of divided word lines of each of the km memory cell array blocks;

arranging km of xy address word lines above or below the km memory cell array blocks; and

arranging km of divided y address word lines vertically connected from each of the km of xy address word lines on a left or a right side of each of the km

memory cell array blocks.

5. A layout method of a semiconductor memory device, comprising:

arranging km memory cell array blocks divided by x block selecting signals and y block selecting signals in the form of a k×m matrix, arranging horizontally a plurality of main word lines of the km memory cell array blocks, arranging vertically a plurality of bit lines, and arranging horizontally a plurality of divided word lines of each of the km memory cell array blocks;

arranging horizontally m of xy address word lines of m memory cell array blocks horizontally arranged among the km memory cell array blocks above or below m memory cell array blocks arranged horizontally; and

arranging vertically y address word lines of each of the km memory cell array blocks connected to xy address word lines of each of the km memory cell array blocks on a left or a right side of each of the km memory cell array blocks.

6. The layout method of claim 5, wherein the y block selecting signals are vertically arranged collectively on a right or a left side of the km memory cell array blocks.

7. The layout method of claim 5, further comprising, arranging, on a right or a left side of the corresponding xy address word lines, a decoding means for decoding a corresponding x block selecting signal among x block selecting signals

generated by decoding the x block address and y block selecting signals generated by decoding the y block address to select the corresponding xy address word lines arranged horizontally above or below each of the km memory cell array blocks.